REMARKS

The above Amendments and these Remarks are in reply to the Office Action mailed June 2, 2005.

Claims 1-6 and 8-26 are currently pending. Applicants have amended claims 1, 8, 9, 11, 15, 16, 17, 19, 23, and 26. Applicants respectfully request reconsideration of claims 1-6 and 8-26.

I. Objection to Claim 11

Claim 11 was objected to because of informalities regarding the phrase, "receiving a plurality of storage input/output requests at least one port." The phrase has been amended to recite "receiving a plurality of storage input/output requests at at least one port." The informalities have been corrected and withdrawal of the objection is respectfully requested.

II. Rejection of Claims 23-26 under 35 U.S.C. § 101

Claims 23-26 were rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter.

The preamble of claim 23 has been amended in accordance with the Examiner's suggestion to recite, "One or more computer-readable media having computer-readable code stored thereon, which when executed by a switch in a storage network causes the switch to perform the following steps." It is respectfully submitted that after amendment, claims 23-26 recite statutory subject matter under 35 U.S.C. § 101. Withdrawal of the rejection under § 101 is requested.

III. Rejection of Claims 11-14 under 35 U.S.C. § 112

Claims 11-14 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, the term "the initiator" was identified as lacking sufficient antecedent basis. Claim 11 has been amended to clarify the term initiator as either a "first initiator" or "second initiator," as recited earlier in the claim. The terms "first initiator" and "second initiator" have

proper antecedent basis in the claim. Accordingly, withdrawal of the rejection of claims 11-14 under 35 U.S.C. § 112, second paragraph is respectfully requested.

There being no outstanding rejections of claims 11-14 under either 35 U.S.C. § 102 or § 103, Applicants respectfully request a notice of allowability as to claims 11-14.

IV. Rejection of Claims 1, 3, and 4 under 35 U.S.C. § 102(a)

Claims 1, 3, and 4 were rejected under 35 U.S.C. § 102(a) as being anticipated by Molero et al. ("On the Switch Architecture for Fibre Channel Storage Area Networks," June 2001), hereinafter referred to as *Molero*. Because *Molero* fails to disclose each limitation of claims 1, 3, and 4, Applicants assert that these claims are patentable over the cited art.

Claim 1 recites, among other limitations:

> the switch including a plurality of ports and a plurality of processing units, wherein each processing unit is associated with at least one port of said plurality of ports to provide load balancing at said at least one port. *Emphasis added.*

As amended claim 1 makes clear, the switch of the system in which the method is performed includes "a plurality of processing units." Each of the processing units is "associated with at least one port" and provides "load balancing at said at least one port." As Applicants describe in their specification, the utilization of multiple processing units allows load balancing to be "done dynamically ... on every port in the switch and for each request by utilizing the SPU processing power on each port." *Specification, p. 43, ¶ 0124 (emphasis added).* Note that SPU referred to in the quote stands for a "storage processing unit."

There is no disclosure in *Molero* of "a plurality of processing units" within a switch as recited in claim 1. The system disclosed in *Molero* simply includes input channels, input buffers, an internal crossbar, a routing and arbitration unit, and output channels. *See Figures 1 and 2, p. 486.* There is nothing that discloses, or even suggests, "a plurality of processing units," as recited in claim 1. *Molero* provides few structural details and even states that the authors of the article "requested architectural switch details from several Fibre Channel manufacturers, but ... this information has not been provided." *Molero, p. 486.*

The Examiner recognized this deficiency of *Molero* in the office action and asserted as inherent that the ports of *Molero* would include respective processing circuitry affiliated with each respective port. Applicants respectfully disagree and assert that such limitations as now recited in claim 1 are in no way inherent in the system or teachings of *Molero*. It is not necessary or inherent for each port of a switch to be associated with a particular processing unit among a plurality of processing units. For example, a switch could include a single central processing unit that is used to process every message at every port. While it may be inherent that messages must have some way of being processed, that fact in no way makes the structure recited in claim 1 inherent.

It is further in no way inherent in *Molero* that individual processing units "provide load balancing at said at least one port," as claim 1 additionally recites. For example, even if there were processing units for each port in *Molero* (a teaching which Applicants maintain is not within *Molero*), the "load balancing" function could still be handled by a central processing unit rather than individual units at each port.

In fact, *Molero* appears to teach centralized processing and load balancing by a single unit rather than a "plurality of processing units," as claim 1 recites. The portions of *Molero* cited for disclosing load balancing teach that the "routing unit iteratively polls input ports, in a round-robin scheduling policy, for new messages that need to be routed. This unit can start routing a message as soon as the header information has arrived." *Molero, p. 436.*

Thus, *Molero* utilizes a single unit – the "routing unit" – for the asserted load balancing. That routing unit is in communication with every input channel and routes the messages received on each input port. *See Molero, Figure 2, p. 486.* Because *Molero* teaches the use of a single "routing unit," *Molero* fails to disclose "a plurality of processing units, wherein each processing unit is associated with at least one port of said plurality of ports to provide load balancing at said at least one port," as recited in claim 1.

Because *Molero* fails to disclose each limitation of claim 1, Applicants assert that claim 1 is patentable over the cited art. Claims 3 and 4 each ultimately depend from claim 1, and therefore, should be patentable for at least the same reasons as claim 1.

V. Rejection of Claims 2, 5, 6, 8-10, and 15-26 under 35 U.S.C. § 103(a)

Claims 2, 5, 6, 8-10, and 15-26 were rejected under 35 U.S.C. 103(a) as being unpatentable over *Molero* in view of U.S. Patent No. 6,324,580 (hereinafter *Jindal*), and further in view of U.S. Patent No. 5,721,904 (hereinafter *Ito*). Because *Molero, Jindal,* and *Ito*, either alone or in combination, fail to teach or suggest each of the limitations of claims 2, 5, 6, 8-10, and 15-26, Applicants assert that these claims are patentable over the cited art.

Claims 8-10

Claims 8 and 9 recite, among other limitations:

> the switch including a plurality of ports and a plurality of processing units, wherein each processing unit is associated with at least one port of said plurality of ports to provide load balancing at said at least one port.

As shown above with respect to claim 1, *Molero* fails to disclose a switch including a "plurality of processing units" that are each "associated with at least one port of said plurality of ports to provide load balancing at said at least one port," as also recited in independent claims 8 and 9. Applicants further assert that *Molero* fails to teach or suggest these limitations. As discussed, *Molero* utilizes a single unit – "the routing unit" – to iteratively poll "the ports, in a round robin scheduling policy, for new messages that need to be routed." *Molero, p. 486.* Nothing within the limited disclosure of *Molero* would suggest to alter the described system to include "a plurality of processing units" with each processing unit "associated with at least one port" of the switch. *Molero* teaches the use of centralized processing of all messages by a single unit rather than processing by individual processing units for different ports. Further, nothing within *Molero* suggests that load balancing be performed by individual processing units associated with the ports rather than a single routing unit as disclosed.

Jindal and *Ito* similarly fail to teach or suggest a switch including a "plurality of processing units" that are each "associated with at least one port of said plurality of ports to provide load balancing at said at least one port." *Jindal* simply teaches a method for directing clients to replicated services. *See e.g., col. 5-6. Jindal* provides little detail as to the structure of the "nameserver" that is

involved in the method. There is nothing that would suggest to one of ordinary skill to use "a plurality of processing units" associated with individual ports to "provide load balancing at said at least one port," as claims 8 and 9 recited. Quite simply, the hardware for routing and load balancing is not described in *Jindal*. *Ito* also fails to teach or suggest these limitations. *Ito* simply discloses a "database access system" and is cited for disclosing the selection of targets based on average response times. Nothing within these teachings addresses or suggests the use of a "plurality of processing units" associated with individual ports for load balancing as recited in claims 8 and 9.

In any combination, *Molero*, *Jindal*, and *Ito* fail to teach or suggest the limitations recited above. Nothing within *Jindal's* description of a method for directing clients to replicated services would suggest to one of ordinary skill to modify the switch disclosed in *Molero* to utilize "a plurality of processing units" rather than the single routing unit described therein. The addition of *Ito* to the combination also fails to make such a suggestion. Taken alone or in combination, nothing within the teachings of the references or knowledge available to one of ordinary skill in the art would lead one to modify the cited references to arrive at the particular structure recited in claims 8 and 9.

Because the cited art, either alone or in combination, fails to teach or suggest each of the limitations of claims 8 and 9, Applicants assert that these claims are patentable under 35 U.S.C. § 103(a). Claim 10 depends from claim 9 and therefore, should be patentable for at least the same reasons.

Claims 15-26

Claim 15 recites:

> a plurality of processing units, wherein each processing unit is associated with one or more ports of said plurality of ports and determines, for storage level input/output requests received at said one or more ports, a respective average response time for each of a plurality of storage input/output paths between the switch and the target.

Claim 17 recites:

> a plurality of processing units, wherein each processing unit is associated with one or more ports of said plurality of ports to provide load balancing at said one or more ports.

Claim 19 recites:

> a switch including a plurality of ports and a plurality of processing units, wherein each processing unit is associated with at least one port to provide load balancing at said at least one port.

Claim 23 recites:

> said switch including a plurality of ports and a plurality of processing units, wherein each processing unit is associated with at least one port of said plurality of ports to provide load balancing at said at least one port.

Each of independent claims 15, 17, 19, and 23 recites similar limitations to those discussed above with respect to claims 1, 8, and 9. Accordingly, for at least the same reasons as claims 1, 8, and 9, Applicants assert that claims 15, 17, 19, and 23 are patentable over the cited art. Claims 16, 18, 20-22, and 24-26 each ultimately depend from one of claims 15, 17, 19, and 23 and therefore, should be patentable for at least the same reasons.

VI. Conclusion

Based on the above amendments and these remarks, reconsideration of claims 1-6 and 8-26 is respectfully requested.

The Examiner's prompt attention to this matter is greatly appreciated. Should further questions remain, the Examiner is invited to contact the undersigned attorney by telephone.

Enclosed is a PETITION FOR EXTENSION OF TIME UNDER 37 C.F.R. § 1.136 for extending the time to respond up to and including today, November 2, 2005.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 501826 for any matter in connection with this response, including any fee for extension of time, which may be required.

Respectfully submitted,

Date: November 2, 2005

By: _____
David E. Cromer
Reg. No. 54,768

VIERRA MAGEN MARCUS HARMON & DENIRO LLP
685 Market Street, Suite 540
San Francisco, California 94105-4206
Telephone: (415) 369-9660
Facsimile: (415) 369-9665